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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/975,293	10/11/2001	Max M. Yeung	01-3221496.00144	1284
24319	7590	09/06/2005	EXAMINER	
LSI LOGIC CORPORATION 1621 BARBER LANE MS: D-106 MILPITAS, CA 95035			TORRES, JOSEPH D	
		ART UNIT	PAPER NUMBER	
		2133		

DATE MAILED: 09/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/975,293	YEUNG ET AL.
	Examiner	Art Unit
	Joseph D. Torres	2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 01 August 2005.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) _____ is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) 1-23 are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5) Notice of Informal Patent Application (PTO-152)

6) Other: _____.

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

- I. Claims 1-13 and 21, drawn to An apparatus for memory error control coding comprising a bypass circuit comprises one or more logic gates configured to (i) receive said first syndrome signal at a first input, (ii) receive said bypass signal at a second input and (iii) present said second syndrome signal at an output, classified in class 714, subclass 763.
- II. Claims 14-20, drawn to An apparatus for memory error control coding comprising a bypass signal, wherein (i) each bit of said second syndrome signal has a state determined by a corresponding bit of said first syndrome signal when said bypass signal is in a first state and (ii) all bits of said second syndrome signal have the same state when said bypass signal is in a second state, classified in class 714, subclass 774.
- III. Claims 22 and 23, drawn to a syndrome encoder circuit configured to generate a syndrome signal in response to a read data signal and a read parity signal, wherein said syndrome encoder circuit comprises a type of syndrome encoder selected from the group consisting of (i) noninverting exclusive-OR gates with an output inverted by a NOT gate, (ii) inverting exclusive-OR gates, (iii) inverting exclusive-OR gates with an output inverted by a NOT gate, (iv) non-inverting exclusive-NOR gates, (v) non-

inverting exclusive-NOR gates with an output inverted by a NOT gate, (vi) inverting exclusive-NOR gates, and (vii) inverting exclusive-NOR gates with an output inverted by a NOT gate, classified in class 714, subclass 785.

The inventions are distinct, each from the other because of the following reasons:

Inventions Group I and group II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group I has separate utility such as for a a bypass circuit comprises one or more logic gates configured to (i) receive said first syndrome signal at a first input, (ii) receive said bypass signal at a second input and (iii) present said second syndrome signal at an output. In the instant case, invention Group II has separate utility such as for a bypass signal, wherein (i) each bit of said second syndrome signal has a state determined by a corresponding bit of said first syndrome signal when said bypass signal is in a first state and (ii) all bits of said second syndrome signal have the same state when said bypass signal is in a second state. See MPEP § 806.05(d).

Inventions Group I and Group III are related as combination (Group I) and subcombination (Group III). Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination (Group I) as claimed does not require the particulars of the subcombination

(Group III) as claimed because syndromes can be generated in software without the use of one of the following (i) noninverting exclusive-OR gates with an output inverted by a NOT gate, (ii) inverting exclusive-OR gates, (iii) inverting exclusive-OR gates with an output inverted by a NOT gate, (iv) non-inverting exclusive-NOR gates, (v) non-inverting exclusive-NOR gates with an output inverted by a NOT gate, (vi) inverting exclusive-NOR gates, and (vii) inverting exclusive-NOR gates with an output inverted by a NOT gate. The subcombination (Group III) has separate utility such as in a standard error correction device where only one syndrome generator is required.

Inventions Group II and Group III are related as combination (Group II) and subcombination (Group III). Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination (Group II) as claimed does not require the particulars of the subcombination (Group III) as claimed because syndromes can be generated in software without the use of one of the following (i) noninverting exclusive-OR gates with an output inverted by a NOT gate, (ii) inverting exclusive-OR gates, (iii) inverting exclusive-OR gates with an output inverted by a NOT gate, (iv) non-inverting exclusive-NOR gates, (v) non-inverting exclusive-NOR gates with an output inverted by a NOT gate, (vi) inverting exclusive-NOR gates, and (vii) inverting exclusive-NOR gates with an output inverted by a NOT gate. The subcombination (Group III) has separate utility

such as in a standard error correction device where only one syndrome generator is required.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group I, II and III are mutually exclusive, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

A telephone call was made to Robert Miller on 825/2005 to request an oral election to the above restriction requirement, but did not result in an election being made.

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

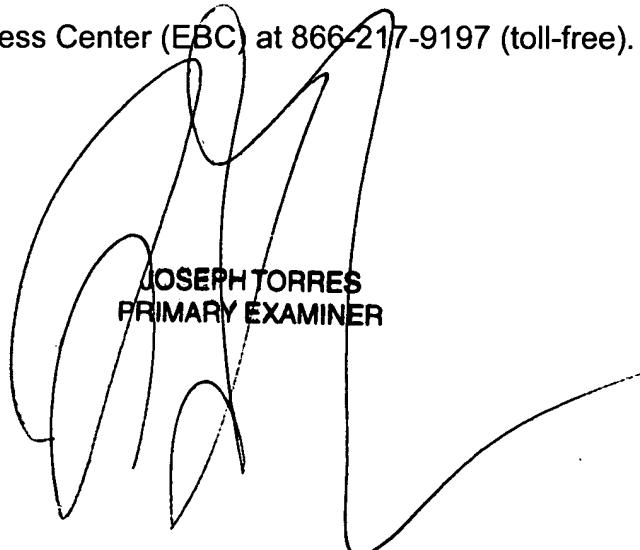
Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decay can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Joseph D. Torres, PhD
Primary Examiner
Art Unit 2133



JOSEPH TORRES
PRIMARY EXAMINER

A handwritten signature of Joseph D. Torres is written over a large, stylized, cursive outline of the same name. The signature is in black ink and is positioned to the right of the stylized name.